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Controlable diffusion parameters with chemical vapour deposition for p–n junction silicon solar cells

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The chemical vapour deposition technique for the fabrication of p–n junction silicon solar cells is reported. This technique involves the use of native oxide on silicon to limit the diffusion flux and yields lower surface concentrations of impurities and shallow p–n junctions. Photolithography is used for cell fabrication. Data are given to demonstrate the effects of technological parameters on solar cell performance and the controllability of the diffusion parameters obtained by this technique.

1. Introduction

In the conventional preparation of a photovoltaic solar cell, a p–n junction is formed by a standard high-temperature diffusion of either boron or phosphorus into a silicon-base material. In order to improve the efficiency, a separate step is required which is the application of a quarter-wave optical thickness antireflective film to the surface of the cell. Such optical coatings are applied by vacuum deposition, sputtering, or other techniques.

During the last decade, industry's interest has grown immensely in doped oxides (silica) films as diffusion sources in electronic device applications [1–5]. This type of diffusion appears to hold several advantages over standard high-temperature deposition and diffusion processes, which include: (a) better overall process control, (b) increased flexibility in choosing diffusion schedules, doping level and device configuration.

In this work we studied the application of silica diffusion sources to solar cell fabrication. The effect of the undoped silicon dioxide layer grown during the cleaning process on the calculation of junction depth was reviewed. The chemical vapour deposition (CVD) technique was used in the fabrication of p–n junction silicon solar cells. Phosphorus-doped oxides were deposited by oxidation of silane and phosphine at a substrate temperature of 350° C. This step was followed by the deposition of the undoped oxide. The overall oxide layer thickness was adjusted to form an antireflective film on the surface of the cell. Experimental data are presented to demonstrate the controllability obtained from CVD silica film application to solar cells.

2. Junction-depth calculations

Consider the schematic representation, shown in Fig. 1, of the different layers and their corresponding parameters. The thickness of the doped oxide, x_0, (with initial concentration C_0) is so thick that no exhaustion is expected during the diffusion time. The undoped oxide of thickness x_B acts as a barrier to diffusion. The diffusion equations in each region can be written as

$$\frac{\partial C_1(x, t)}{\partial t} = D_1 \frac{\delta^2 C_1(x, t)}{\partial x^2}$$

$$-x_0 < x < -x_B, \quad t > 0 \tag{1}$$

$$\frac{\partial C_2(x, t)}{\partial t} = D_2 \frac{\partial^2 C_2(x, t)}{\partial x^2}$$

$$x > 0, \quad t > 0 \tag{2}$$

$$\frac{\partial C_3(x, t)}{\partial t} = D_3 \frac{\partial^2 C_3(x, t)}{\partial x^2}$$

$$-x_B < x < 0, \quad t > 0 \tag{3}$$

where D_1, D_2 and D_3 are the diffusion coefficients in the doped, undoped and semiconductor regions, respectively. C_1, C_2, C_3 are the doping concentration in the same regions, respectively.

Assuming the diffusion constants are not functions of concentration and ignoring any field-aided diffusion terms operating on ionized dopants, the

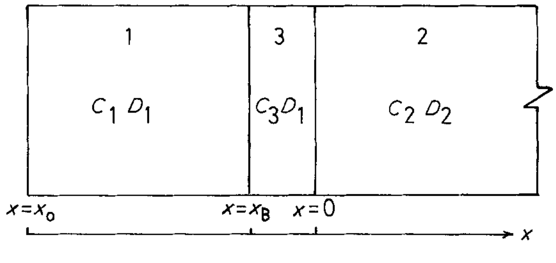

Figure 1 Layer structure with diffusion parameters.

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appropriate boundary conditions are

$$C_1 = C_0, \qquad (4)$$

$$C_2 = C_3 = 0 \qquad \text{at } t = 0$$

$$C_1 = 0 \qquad \text{at } x = -x_0, \quad t > 0 \qquad (5)$$

$$C_2 \rightarrow 0 \qquad \text{as } x \rightarrow \infty, \quad t > 0 \qquad (6)$$

$$C_3 = C_1 \qquad \text{at } x = -x_B, \quad t > 0 \qquad (7)$$

$$D_1 \frac{\partial C_1}{\partial x} = D_1 \frac{\partial C_3}{\partial x} \qquad \text{at } x = -x_B, \quad t > 0 \qquad (8)$$

$$C_2 = m \quad C_3, \qquad \text{at } x = 0, \quad t > 0 \qquad (9)$$

$$D_1 \frac{\partial C_3}{\partial x} = D_2 \frac{\partial C_2}{\partial x} \qquad \text{at } x = 0, \quad t > 0 \qquad (10)$$

where m, the segregation coefficient, defines the ratio of dopant concentration in silicon to that in the oxide at the silicon–oxide interface.

Considering the constant source condition of doped oxides, the solution for the concentration in silicon is reduced to a simple form [6]

$$C_2(x, t) = \frac{C_0(D_1/D_2)^{1/2}}{1 + K} \operatorname{erfc} \frac{x_B + mkx}{2(D_1 t)^{1/2}} \qquad (11)$$

where t is the diffusion time, and

$$k = \frac{1}{m}(D_1/D_2) \qquad (12)$$

If $(1/m)\,(D_1/D_2)^{1/2}$ is small compared to unity (and this appears to be the case for both boron and phosphorus in silicon), then Equation 11 becomes

$$C_2(x, t) = C_0\left(\frac{D_1}{D_2}\right) \operatorname{erfc} \frac{x_B(D_2/D_1)^{1/2} + x}{2(D_2 t)^{1/2}} \qquad (13)$$

In order to calculate the junction depth, x_j, we apply Equation 13 to the two cases below.

2.1. Case (i), no undoped barrier

In this case, Equation 13 reduces to the simple case of diffusion from a semi-infinite source into a semi-infinite sink, which is complementary-error-function with an equivalent surface concentration, C_s given by

$$C_s = C_0\left(\frac{D_1}{D_2}\right)^{1/2} \qquad (14)$$

Thus, the surface concentration of this simple case is independent of time and the junction depth can be written as

$$x_{jN} = 2\,(D_2 t)^{1/2} \arg \operatorname{erfc}\left[\frac{C_B}{C_0}\left(\frac{D_2}{D_1}\right)^{1/2}\right] \qquad (15)$$

where C_B is the bulk concentration of the substrate.

2.2. Case (ii), undoped barrier oxide included

In this case, the surface concentration is given by

$$C_s = C_0\left(\frac{D_1}{D_2}\right)^{1/2} \operatorname{erfc}\left[\frac{x_B}{(2D_1 t)^{1/2}}\right] \qquad (16)$$

which is now time dependent.

The junction depth in the presence of the barrier oxide, x_{jB}, is

$$x_{jB} = -x_B\left(\frac{D_2}{D_1}\right)^{1/2} + 2\,(D_2 t)^{1/2} \arg \times \operatorname{erfc}\left[\frac{C_B}{C_0}\left(\frac{D_2}{D_1}\right)^{1/2}\right] \qquad (17)$$

3. Optimum diffusion parameters for solar cells

As the diffusion process is the most critical step in the fabrication of solar cells, several diffusions were devoted in order to control the technological parameters (junction depth, sheet resistance, ...) in the diffused region of the cell. The diffusions were carried out at 950° C for 30 min in a nitrogen ambient; the pulling rate of the wafer after diffusion was $20\,\text{cm}\,\text{min}^{-1}$. Table I summarizes some technological parameters of these diffusions. Variations in doped and undoped silicon dioxide deposition time have taken place. The undoped oxide serves as a protection layer for the phosphorus out-diffusion as well as good adhesion for the application of photoresist material for later processes. The importance of total silicon dioxide thickness measurements lies in using it as an antireflection coating, so a thickness of 350 nm was deposited for all our cells. It is known that in order to minimize the recombination losses and to improve the photocurrent of the solar cell, we have to decrease the junction depth and lower the doping level. So we can deduce from Table I that the junction depths and the sheet resistances corresponding to $0.3\,\text{l}\,\text{min}^{-1}$ phosphine flow rate are convenient for solar cell fabrication.

4. Technology

The starting material used throughout this study was

TABLE I Some technological parameters

Wafer no.	Deposition time (min)		Phosphine flow rate ($\text{l}\,\text{min}^{-1}$)	Junction depth (μm)	Sheet resistivity ($\Omega\,\text{cm}^{-1}$)
	Doped	Undoped			
1	2	1.7	0.25	0.2	203
2	2	2	0.3	0.58	56
3	1.5	2	0.3	0.25	100
4	1.5	2.3	0.35	0.5	43
5	2	1.7	0.3	0.42	57
6	2	2.0	0.3	0.5	54
7	2.5	2.5	0.3	0.43	50

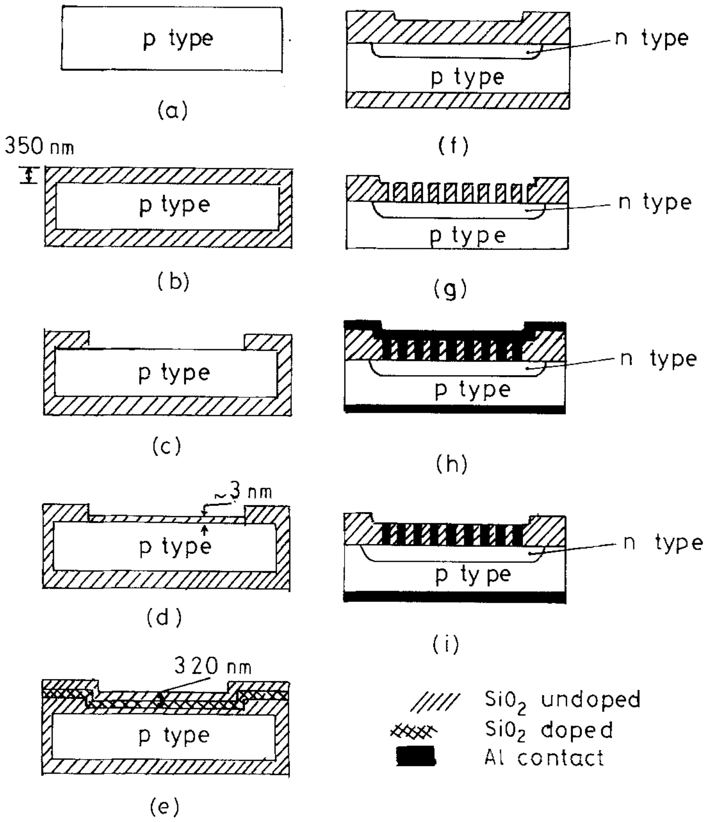


Figure 2 Fabrication processes (a) p-type silicon wafer, (b) thermal oxidation, (c) front layer guard ring, (d) chemical oxidation, (e) CVD process, (f) drive-in diffusion, (g) etching of contact windows, (h) metallization process, (i) etching of aluminium.

a p-type boron-doped Wacker monocrystalline silicon wafers with one side polished and the other side lapped, resistivity 1.8 to 2.4 Ωcm, diameter 5.7 cm (2$\frac{1}{4}$ in.), thickness 400 μm, orientation (1 0 0). The specific resistivity of each wafer was determined by four-point probe and the dopant concentration was calculated. The technological steps are shown in Fig. 2.

4.1. Cleaning process

The pretreatment of the wafers comprised:

(a) 2 min trichlorothylene, 2 min propanol in order to remove greasy films;

(b) 10 min fuming nitric acid in order to remove ionic contaminants;

(c) boiling 10 min in 3:1 hydrochloric acid : nitric acid in order to remove metallic deposits.

Deionized water rinse for a 5 to 10 min and spin drying followed each acid treatment.

4.2. Thermal oxidation process

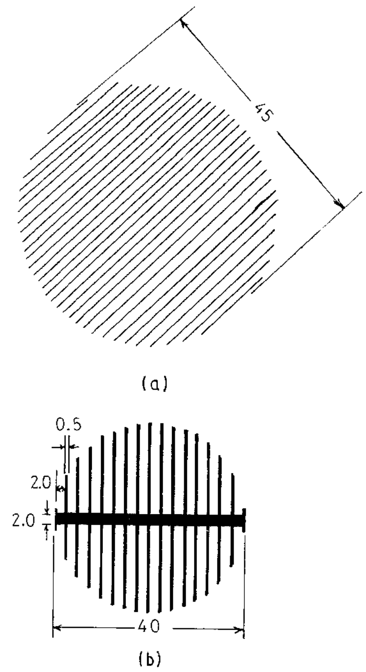
The wafers were oxidized at 950° C in an atmosphere of oxygen containing water vapour for 70 min, followed by dry oxygen for 5 min. Layers of silicon dioxide of thickness 320 nm were produced by this procedure.

4.3. Front-layer guard ring

In order to minimize the surface leakage of the cells, a guard ring was made around the front surface by photolithography using a mask shown in Fig. 3. This is done by applying a negative photoresist HR 100 (Waycoat) on both sides of the wafer, spun at 6000 r.p.m. for 20 sec (we applied the photoresist first on the back surface, baking it for 2 min at 70° C, then on the front surface, prebaked at 70° C for 15 min, exposed to ultraviolet light for 2 sec through the mask for the front surface and direct exposure for the back surface) developing in xylene for 2 min, fixing in propanol for 2 min, rinsing in de-ionized (DI) water, postbacking at 120° C for 15 min. The front layer was etched in SiO$_2$ etchant (NH$_4$F, 58 g, HF (40%) 27 ml DI water 69 ml) for 3 min, rinsed in DI water for 5 min. The remaining photoresist on the quard ring and back layer was removed by fuming nitric acid treatment for 10 min, rinsed in water then spin dried. The thin SiO$_2$ layer which is grown in this step is used as a retarding mechanism (diffusion limiting due to oxidation).

4.4. Chemical vapour deposition (CVD) process

The depositions were performed in a home-made one-



(a)

(b)

Figure 3 (a) Guard ring mask. (b) Front layer contact mask.

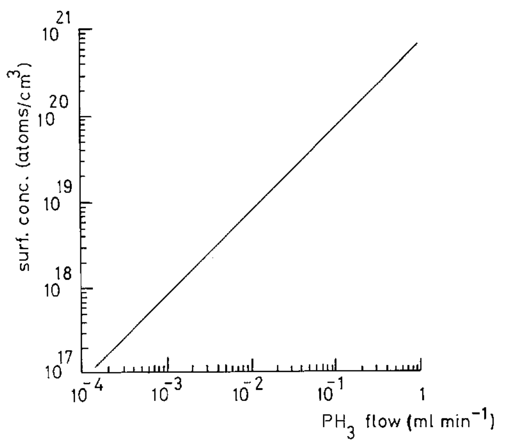


Figure 4 Principal stresses of rigid inclusion.

silica reactor [6] at 350° C. Before deposition the reactor was purged with nitrogen and the water preheated for 2 min, the gas flow rates were: $0.1\,\mathrm{l\,min^{-1}}$ oxygen, $0.7\,\mathrm{l\,min^{-1}}$ silane (1% in argon), phosphine + argon $8.5\,\mathrm{l\,min^{-1}}$. The deposition rate was $80\,\mathrm{nm\,min^{-1}}$.

First a uniform phosphorus-doped oxide layer was deposited followed by an undoped oxide layer. A surface concentration of $1 \times 10^{20}\,\mathrm{cm^{-3}}$ was obtained from the experimental curve shown in Fig. 4 [7] at a phosphine flow rate of $0.3\,\mathrm{l\,min^{-1}}$ (2000 p.p.m.).

4.5. Drive-in diffusion process

The diffusions were carried out in pure nitrogen at a flow rate of $1\,\mathrm{l\,min^{-1}}$. The diffusion parameters, e.g. diffusion-time, diffusion temperature, the pulling rate of the wafer from the furnace, were varied according to the improvement in solar cell performance. In order to avoid the introduction of contamination into the furnace during moving the wafer into and out of the furnace, the nitrogen flow rate was raised to $2\,\mathrm{l\,min^{-1}}$.

4.6. Etching of contact windows

Photolithography (See section 4.3) was repeated using the front contact mask shown in Fig. 3. The contact windows were obtained by etching in SiO$_2$.

4.7. Contacts

Aluminium contacts were deposited in an Edward 306E vacuum system at 10^{-6}torr. The wafer was dipped in HF (4%) (HF (40%) 10 ml, DI water 90 ml) for 5 sec, rinsed in DI water and spin dried. The wafer was directly placed into the evaporator. Metallization was carried out first on the front layer of the wafer then on the back layer; the aluminium thickness was about 1 μm. Positive photoresist Az 1350 (Shiply) was applied on both sides of the wafer, spun at 4500 r.p.m. for 20 sec (as noted in the producer's information), prebaked at 70° C for 15 min. The photoresist application was carried out first on the back side followed by baking for 2 min at 70° C, then on the front side of the wafer, prebaked at 70° C for 15 min. The front side was then exposed to ultraviolet light for 4 sec through the contact mask, developed in AZ developer for 2 min, rinsed in water as a stopper for 2 min, centrifuged, and postbaked for 15 min. The wafer was dipped in aluminium etchant phosphoric acid (85%) 150 ml, acetic acid (100%) 30 ml, nitric acid (65%) 10 ml, DI water 30 ml for 3 min, at 40° C, rinsed in DI water for 5 min. The remaining photoresist was removed by immersing the wafer in fuming nitric acid for 10 min, rinsing in DI water for 10 min and spin drying.

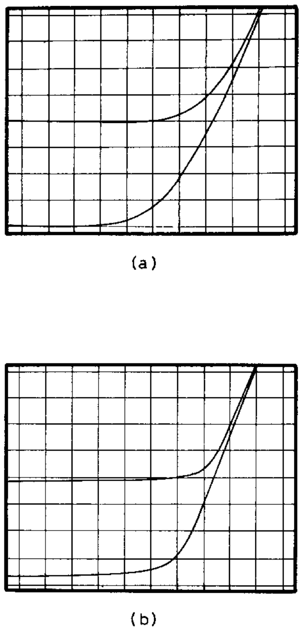


Figure 5 I–V characteristics of series 1 solar cells. V = 0.2 V/div., and I = 50 mA/div.

The cell was sintered (both the front and back contacts at the same time) at 450° C for 10 min in hydrogen ambient.

5. Solar cell fabrication and results

Two sets of solar cells were fabricated according to the results of Section 4 and tested. A comparison was made between our cells and commercial cells exposed to the same illumination level. Set 1, as shown in Fig. 5, were inefficient having fill factors averaging 0.40. This low value of fill factor may be due to the high series resistance (2.5 Ω) which is in turn due to the easy penetration of the metallization through the shallow junction depth. The small short circuit current may be explained by its short lifetime as a result of high pulling rate ($20\,\mathrm{cm\,min^{-1}}$) of the wafer from the furnace after diffusion.

The solar cells of set 2 were fabricated with a longer diffusion time (1 h) in order to obtain relatively deeper junction depths. Fig. 6 shows the variation of the junction depth with diffusion time. From this figure it is clear that the undoped oxide layer on the silicon

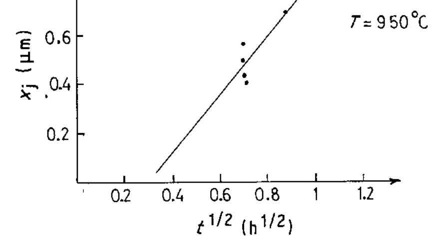


Figure 6 Variation of junction depth with diffusion time.

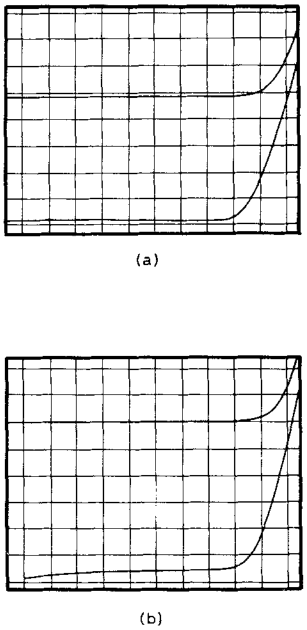


Figure 7 I–V characteristics of series 2 solar cells. $V = 0.1\,\mathrm{V/div.}$, and $I = 50\,\mathrm{mA/div.}$

surface, which must be penetrated in a finite amount of time, acts as a retarding diffusion mechanism on the substrate. The characteristics shown in Fig. 7 are obtained for cells having fill factors averaging 0.72 and pulling rate $\sim 5\,\mathrm{cm\,min^{-1}}$. The cell parameters are: (i) junction depth $0.8\,\mu\mathrm{m}$, (ii) sheet resistance $25\,\Omega/\square$, (iii) series resistance $0.3\,\Omega$ and (iv) shunt resistance $2\,\mathrm{k}\Omega$.

6. Conclusions

A chemical vapour deposition technique for fabricating solar cells is presented. The technological processes using photolithography are described in detail. The solar cells processed by this technique have good characteristics. Their series resistances are comparable to commercial ones. These improvements are due to the uniformity of the silica film which leads to a homogeneous surface concentration approximately equal to $1 \times 10^{20}\,\mathrm{cm^{-3}}$ for a phosphine flow rate $0.3\,\mathrm{l\,min^{-1}}$, and a shallow uniform junction. The process control can be achieved by varying the phosphine flow rate and the deposition time of doped and undoped silica film. The calculations of the junction depth have been performed, and a phenomenon of a retarding mechanism due to the silicon dioxide film initially present on the silicon wafer during the cleaning process, has been found.

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References

1. M. L. BARRY and P. OLSEN, *Solid State Technol.* **11** (1968) 39.
2. *Idem, J. Electrochem. Soc. Solid State Sci. Technol.* **116** (1969) 258.
3. *Idem, ibid.* **117** (1970) 1905.
4. K. M. MAR, *ibid.* **126** (1979) 1252.
5. D. L. FLOWERS and SCHYI-YI WU, *ibid.* **129** (1982) 229.
6. C. J. P. PEIJNEN, P. A. JANSEN, J. F. G. J. OLIJSLAGERS and W. VERSNEL, Eindhoven University of Technology, EVT Report 81-E-119, ISBN 90-6144-119-6 (1981).
7. C. J. H. HEIJEN and B. H. VAN ROY, Eindhoven University of Technology EVT Report 83-E-133, ISBN90-133-1, ISSO167-9708 (1983).

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